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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/527,575	03/14/2005	Frederic Claude Marie Piry	550-625	9134

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EXAMINER	
FAHERTY, COREY S	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/527,575	PIRY, FREDERIC CLAUDE MARIE	
	Examiner	Art Unit	
	Corey S. Faherty	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the reply filed 03/15/2007.

2. Claims 1-26 are pending in the application and have been examined.

Specification

3. The specification has been amended to correct minor typographical errors. No new matter has been added, and the amendments to the specification are therefore accepted.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5, 11, 14-18 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Song et al. (*The PowerPC 604 RISC Microprocessor*), referenced from here forward as Song.

6. Regarding claims 1 and 14, Song discloses an apparatus for processing data under control of data processing instructions specifying data processing operations, said apparatus comprising: a first execution mechanism configured to execute a first set of data processing instructions [page 13, Figure 4; Integer Unit 1]; a second execution mechanism configured to execute a second set of data processing instructions [page 13, Figure 4, Integer Unit 2], said first set of data processing instructions overlapping with said second set of data processing instructions such that

one or more data processing instructions are executable by either said first execution mechanism or said second execution mechanism [page 13, first column, lines 5-7; integer units execute all other integer instructions]; and an execution mechanism selector configured to pseudo randomly select either said first execution mechanism or said second execution mechanism to execute one or more data processing instructions that are executable by either said first execution mechanism or said second execution mechanism [page 11, Figure 3; page 11, first column, *Instruction decode and dispatch*; the dispatch logic dispatches instructions to the execution units, including the two integer units; the selection of the first or second integer unit is based in part on resource availability, which is a pseudo random event because it depends on a large number of unpredictable events, such as asynchronous interrupts and user input; interrupts are described further on page 9, first column]; wherein said execution mechanism selector is configured to be controlled by a pseudo random execution mechanism selecting signal generated by a pseudo random signal generator [the dispatch logic uses pseudo random inputs such as asynchronous interrupts and user input to determine which integer unit will be used for each instruction].

7. Regarding claims 2 and 15, Song discloses the apparatus as claimed in claim 1 and the method as claimed in claim 14, wherein said first execution mechanism and said second execution mechanism have at least one different execution characteristic for at least one of said data processing instructions that are executable by either said first execution mechanism or said second execution mechanism [page 12, first column, *Reservation stations and result forwarding*; each execution unit has a reservation station where dispatched instructions wait to be executed; depending on other instructions that are in the reservation station, the instruction could be issued immediately out-of-order or it may have to wait until other instructions finish executing].

8. Regarding claims 3 and 16, Song discloses the apparatus as claimed in claim 2 and the method as claimed in claim 15, wherein said at least one different execution characteristic includes one or more of: time to execute said data processing instruction [page 12, first column, *Reservation stations and result forwarding*; instruction could be issued immediately or have to wait depending on other instructions that are in the reservation station]; and power consumption when executing said data processing instruction [page 12, first column, *Reservation stations and result forwarding*; the power consumption for an instruction which issues out-of-order will be different than for one which issues in-order].

9. Regarding claims 4 and 17, Song discloses the apparatus as claimed in claim 2 and the method as claimed in claim 15, wherein at least one execution characteristic of at least one data processing instruction executed by one of said first execution mechanism or said second execution mechanism varies in dependence upon whether a preceding data processing instruction was executed with either said first execution mechanism or said second execution mechanism [page 12, first column, paragraph 3; the dispatch logic uses resource availability as a method for determining which execution unit to dispatch instructions to, and resource availability depends on instructions that were previously issued to the execution units].

10. Regarding claims 5 and 18, Song discloses the apparatus as claimed in claim 1 and the method as claimed in claim 14, wherein all of said data processing instructions are executable by either said first execution mechanism or said second execution mechanism [page 13, first column, lines 5-7; integer units execute all other integer instructions].

11. Regarding claims 11 and 24, Song discloses the apparatus as claimed in claim 1 and the method as claimed in claim 14, comprising a processor core [page 13, Figure 4; page 12, first

column, *Reservation stations and result forwarding*; integer units and reservation stations], said pseudo random execution mechanism selecting signal being an input to said processor core [page 9, first column, *Precise interrupts and register renaming*; page 12, first column, paragraphs 2-5; instruction dispatch is determined by many pseudo random factors exterior to the processor core, including asynchronous interrupts and user input].

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. Claims 6-10, 12-13, 19-23 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song as applied to claims 1 and 14 above, and further in view of Lindwer (U.S. Patent 6,298,434).

15. Regarding claims 6 and 19, Song does not disclose that the first execution unit is operable to execute some instructions as native instructions and the remaining instructions using emulation software.

Lindwer discloses a processor having a preprocessor and an execution core which together comprise an execution unit capable of executing some instructions as native instructions and the remaining instructions using emulation software [col. 2, lines 27-47].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable both execution units in Song to execute some instructions as native instructions and the remaining instructions using emulation software because Lindwer discloses an execution unit that does this [col. 2, lines 27-47] and teaches that it gives the processor more flexibility [col. 2, lines 17-19] and saves clock cycles during execution [col. 2, lines 43-44].

16. Regarding claims 7 and 20, Song does not disclose that the second execution unit is operable to execute all of the instructions using emulation software.

Lindwer discloses a processor having a preprocessor and an execution core which together comprise an execution unit capable of executing some instructions as native instructions and the remaining instructions using emulation software [col. 2, lines 37-47].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to enable both execution units in Song to execute some instructions as native instructions and the remaining instructions using emulation software because Lindwer discloses an execution unit that does this [col. 2, lines 27-47] and teaches that it gives the processor more flexibility [col. 2, lines 17-19] and saves clock cycles during execution [col. 2, lines 43-44]. In this processor, all virtual instructions are processed using emulation software [Lindwer, col. 2,

lines 31-35], so a program having only virtual instructions could be executed using only emulation software.

17. Regarding claims 8 and 21, Song in view of Lindwer discloses the apparatus as claimed in claim 6 and the method as claimed in claim 19, wherein said first execution mechanism and said second execution mechanism share at least some emulation software [Lindwer, col. 2, lines 17-19, 43-44; allowing execution units to execute some instructions as native instructions and the remaining instructions using emulation software gives a processor more flexibility and saves clock cycles during execution; Song, page 8, first column, *Performance strategy*; page 13, Figure 4; using multiple execution units of the same type in parallel improves performance; two identical execution units of the type described in Lindwer would use the same emulation software and would improve performance].

18. Regarding claims 9 and 22, Song does not specifically disclose processing Java bytecode instructions, though the practice is well known in the art. Lindwer discloses processing Java bytecode instructions in a processor [col. 10, lines 43-45].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to execute Java bytecode instructions in the processor of Song because the practice of processing Java bytecode instructions in processors was well known in the art [Lindwer, col. 10, lines 43-45].

19. Regarding claims 10 and 23, Song does not disclose that the first execution mechanism includes native instruction execution hardware nor that the second execution mechanism uses Java bytecode emulation for all Java bytecodes.

Lindwer discloses a processor having a first execution unit that executes native instructions [col. 2, lines 45-47; processor core] and a second execution unit that uses software emulation for all Java bytecodes [col. 2, lines 31-35, preprocessor]. Lindwer also teaches motivation for including native Java bytecode execution hardware in the first execution unit, that motivation being that the processor may, in response to a special instruction such as a Java virtual instruction, have the processor core transfer arguments to standard locations and then allow the virtual instruction to execute [col. 11, lines 15-22, 47-56], speeding execution of the virtual instruction.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the first execution unit in the system of Song include native instruction execution hardware and to have the second execution unit in the system of Song use Java bytecode emulation for all Java bytecodes because Lindwer discloses using this method [col. 2, lines 31-35, preprocessor; col. 2, lines 45-47; processor core; col. 11, lines 15-22, 47-56; processor core includes logic for executing native Java bytecodes] and teaches that it gives the processor more flexibility [col. 2, lines 17-19], saves clock cycles during execution [col. 2, lines 43-44] and speeds execution of virtual instructions [col. 11, lines 15-22, 47-56].

20. Regarding claims 12 and 25, Song does not specifically disclose a system configuration parameter operable to force the execution mechanism selector to select the first execution mechanism for all data processing instructions.

Lindwer discloses a system using a configuration register that indicates which of two execution units [col. 2, lines 31-35, preprocessor; col. 2, lines 45-47; processor core] will execute an instruction [col. 5, lines 35-41].

It would have been obvious to one or ordinary skill in the art at the time the invention was made to use a system configuration parameter operable to force the execution mechanism selector in Song to select the first execution mechanism for all data processing instructions because Lindwer discloses doing this [col. 5, lines 35-41] and teaches that it gives the processor more flexibility [col. 2, lines 17-19] and saves clock cycles during execution [col. 2, lines 43-44]. This method also allows an instruction to change the system configuration [col. 5, lines 39-41].

21. Regarding claims 13 and 26, Song in view of Lindwer discloses the apparatus as claimed in claim 12 and the method as claimed in claim 25, wherein said system configuration parameter is stored in a system configuration register [Lindwer, col. 5, lines 35-39].

Response to Arguments

22. Applicant's arguments filed 03/15/2007 have been fully considered but they are not persuasive. Specifically, applicant's arguments that Song does not disclose a pseudo random signal generator are not persuasive. Applicant states that a pseudo random signal generator generates a set of values or elements that is statistically random [page 12, paragraph 2]. However, no such description of a pseudo random signal generator is found in the specification of the application or in the claim itself. Applicant gives an example of a pseudo random signal generator [page 10, line 30], but in no way limits the claim language to such an example. The standard for claim interpretation is to give words their plain meaning unless such meaning is inconsistent with the specification [MPEP 2111.01; *In re Zletz,* 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)]. Furthermore, 37 CFR 1.75(d)(1) clearly states that any terms and phrases used in the claims must find clear support or antecedent basis in the description so that

the meaning of the terms in the claims may be ascertainable by reference to the description. Because no clear definition for the phrase "pseudo random signal generator" is provided in the specification, the phrase is given its plain word meaning. That is, "pseudo random signal generator" is interpreted as any hardware or software component capable of producing a pseudo random output.

The question then becomes: do the "unpredictable events, such as asynchronous interrupts and user input" in the system of Song meet this definition? Applicant states that the signal generator of the invention "is 'pseudo' random because the generation algorithm can, for example, repeat the sequence" [page 12, paragraph 2]. This repetition would cause a pattern to appear in the output of the signal generator. Applicant then argues that the "unpredictable events" interpreted by the examiner to be pseudo random are not actually pseudo random and uses the fact that they could have a pattern as evidence to support this argument [page 12, paragraph 2]. However, from applicant's above definition of what "pseudo random" is, it is clear that not only *can* a pseudo random signal have a pattern, but it *must* have a pattern. For these reasons, applicant's argument that Song does not disclose a pseudo random signal generator is not persuasive.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey S. Faherty whose telephone number is (571) 270-1319. The examiner can normally be reached on Monday-Thursday and every other Friday, 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Corey S Faherty
Examiner
Art Unit 2183

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